REMARKS

The examiner objects to the drawings under 37 C.F.R. § 1.83(a). The examiner indicates the drawings must show every feature of the invention specified in the claims.

The application includes claims 1-4, 7-11 and 16-21 prior to entering this amendment.

The examiner rejects claims 18-21 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement.

The examiner rejects claims 1-4, 7-11 and 18-21 under 35 U.S.C. § 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. §103(a) as being obvious over Godiwala, et al. (U.S. Patent 5,712,858).

The applicant amends claims 1 and 7 and cancels claims 19 and 21. The application remains with claims 1-4, 7-11, 16-18 and 20 after entering this amendment.

The applicant adds no new matter and requests reconsideration.

Examiner Interview

The undersigned and Ayan Paul, a Patent Engineer, had a telephonic interview with examiner Radosevich on 7/5/07 to discuss Godiwala. The participants reached no agreement on allowability of the rejected claims over the reference. The undersigned also requested the examiner to reconsider the finality of the office action.

Finality of the office action

In the immediate previous office action dated 12/20/06, the examiner rejected the claims as being unpatentable over Deb. In a response filed on 3/30/07, the applicant provided arguments to overcome Deb and also amended independent claim 7 (by replacing a "the" in the claim to "a" to correct an antecedent basis problem) to overcome a 112 rejection. In the current office action dated 5/8/07, the examiner rejects the claims in view of a new reference (Godiwala) and argues that the applicant's amendment necessitated the new grounds of rejection and accordingly, makes the current office action final. The applicant believes that the amendment to claim 7 in the response filed on 3/30/07 was merely to correct certain informalities and did not change the scope of the claim. And hence, the finality of the current office action is premature. The applicant, accordingly, requests the examiner to reconsider and withdraw the finality of the office action. MPEP 706.07(d).

Claim Rejections Under §112

The examiner rejects claims 18-21 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The examiner alleges that certain limitations of claim 18 are not supported within the specification, and are thus viewed as new subject matter. The applicant traverses the rejection for the following reasons.

Claim 18 recites *the first group and the second group of output signals are not provided to a second group of data output pins during the first test cycle and the second test cycle of the test mode*. Claim 20 includes similar limitations. The applicant believes that the figures and the specification disclose the recited limitation. For example, in the embodiments of figures 4A and 4B, signals S1, S3, ..., S_{n-1} (i.e., the odd numbered output signals) disclose the recited first group of output signals and signals S2, S4, ..., S_n (i.e., the even numbered output signals) disclose the recited second group of output signals. Additionally, output pins P1, P3, ..., P_{n-1} (i.e., the odd numbered output pins) disclose the recited first group of data output pins and output pins P2, P4,...,P_n (i.e., the even numbered output pins) disclose the recited second group of data output pins. Figures 4A and 4B illustrate the data output paths when the IC is in a test mode.[1] "In FIG. 4A and FIG. 4B, a solid line denotes a data path during a first test cycle and a dotted line denotes a data path during a second test cycle."[2] As illustrated in the figures, the first group of output signals (S1, S3, ..., S_{n-1}) and the second group of output signals (S2, S4, ..., S_n) are not provided to the second group of data output pins (P2, P4,...,P_n) either during the first test cycle (solid lines) or during the second test cycles (dotted lines), as would be required by claims 18 and 20. And hence, the figures and the corresponding disclosure in the specification support the recited limitation. For these reasons, the applicant asks the examiner to remove the rejection to claims 18 and 20.

Drawing Objections

The examiner objects to the drawings under 37 C.F.R. § 1.83(a). The examiner indicates the drawings must show every feature of the invention specified in the claims. In view of the above discussion regarding rejections under § 112, the applicant believes that the objection to the drawings are obviated.

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[1] Specification, page 7, lines 8-9.
[2] Specification, page 7, lines 19-21.

Claim Rejections Under §102 & 103

The examiner rejects claims 1-4, 7-11 and 18-21 as being anticipated by or, in the alternative, obvious over Godiwala. The applicant traverses the rejection for the following reasons.

Godiwala, in figure 2, teaches an electronic test system 12A for testing a device under test DUT 10A that includes contacts C1-C8. The "tester 12A has a probe card 16A that provides split probes 20A, 22A, 24A and 26A."[3] Each of the split probes 20A-26A are connected to two of the output pins C1-C8 of the DUT 10A. For example, split probe 20A is connected to two output pins C1 and C2; and split probe 22A is connected to two output pins C3 and C4.

Claim 1 recites *a plurality of data output pins; ...where a first group of output signals are provided to a first group of data output pins during a first test cycle of the test mode; and where a second group of output signals are provided to the first group of data output pins during a second test cycle of the test mode.* Claim 7 includes similar limitations. The examiner argues that Godiwala's DUT 10A discloses the recited semiconductor circuit and Godiwala's contacts C1-C8 of the DUT 10A disclose the recited data output pins.

The examiner has not specifically identified which of Godiwala's plurality of contacts C1-C8 disclose the recited first group of data output pins. Even if, *arguendo*, one or more of the contacts C1-C8 disclose the recited first group of data output pins, the contacts C1-C8 are not provided with a *first group of output signals* during a first test cycle and a *second group of output signals* during a second test cycle, as would be required by the claims. Rather, Godiwala merely shows two of the output pins (e.g., output pins C1 and C2) of the DUT 10A coupled to a single split probe 20A of the probe card 16A of the tester 12A. Godiwala, thus, fails to disclose a first group of output signals provided to a one or more of the contacts C1-C8 during a first test cycle and a second group of output signals provided to one or more of the contacts C1-C8 during a second test cycle, as recited in claims 1 and 7. And hence, Godiwala's contacts C1-C8 can not disclose the recited first group of data output pins.

Note that the claims recite a *semiconductor integrated circuit comprising: a plurality of data output pins...* That is, the recited data output pins are included in the recited semiconductor integrated circuit. And hence, Godiwala's split probes 20A-26A of the probe card 16A of the tester 12A (which is separate from the DUT 10A) can not possibly disclose the recited data

[3] Godiwala, column 4, line 66 to column 5, line 10.

output pins. This is because the DUT 10A (the alleged semiconductor integrated circuit) does not include the split probes 20A-26A.

Additionally, the applicant amends claims 1 and 7 to include limitations from now canceled claims 19 and 21, respectively. Claim now 1 recites *during the normal mode: the first group of output signals are provided to the corresponding data output pins of the first group of data output pins; and the second group of output signals are provided to the corresponding data output pins of a second group of data output pins.* Claim 7 includes similar limitations. As disclosed before, Godiwala's split probes 20A-26A of the probe card 16A of the tester 12A can not possibly disclose the recited data output pins. Even if, *arguendo*, Godiwala's split probes 20A-26A does disclose the recited data output pins, the split probes 20A-26A are not divided in a first group of data output pins and a second group of data output pins, as would be required by claims 1 and 7. And hence, Godiwala can not disclose the second group of output signals provided to the corresponding split probes of a second group of split probes, as would be required by claims 1 and 7. And finally, the split probes 20A-26A can not operate during a normal mode, as the split probes are included in the probe card of a tester (which inherently operates in a test mode only). For these additional reasons, Godiwala's split probes 20A-26A can not possibly disclose the recited data output pins.

For at least these reasons, independent claims 1 and 7 are allowable, along with their associated dependent claims.

Conclusion

The applicant requests reconsideration and allowances of the remaining claims. The applicant encourages the examiner to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

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Respectfully submitted,

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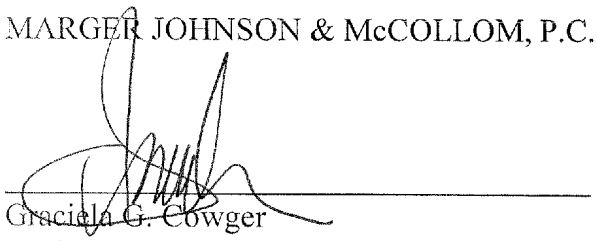

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